REMARKS

In the above-identified Office Action, the Examiner objected to Claims 11 and 16. The Examiner further rejected Claims 1, 6, 11 and 16 under 35 U.S.C. §102(e) as being anticipated by Nakashima. Claims 2 - 5, 7 - 10, 12 – 15 and 17 - 20 were rejected under 35 USC §103(a) as being unpatentable over Nakashima in view of Acharya et al.

Regarding the objection to Claims 11 and 16, the Examiner asserted that the reason for the rejection is because the claims are Jepson claims and are not on a separate sheet or electronic page in accordance with 37 CFR §1.52(b)(3). Applicants respectfully disagree.

37 CFR §1.52(b)(3) states that:

> The application (specification, including the claims, drawings, and oath or declaration) or re-examination proceeding and any amendments or corrections to the application or proceedings.
> (3) The claim or claims must commence on a separate physical sheet or electronic page (§1.72(b)).”

Thus, 37 CFR §1.52(b)(3) only requires that the commencement of the presentation of the claims be on a separate sheet (or electronic page).

The commencement of the presentation of the claims has always been on a separate sheet (see the original Application as well as all Applicants' Responses). Therefore, the claims fall under 37 CFR §1.52(b)(3).

Nonetheless, it should be pointed out that Claims 11 and 16 are not Jepson claims as asserted by the Examiner. A Jepson claim is a claim that admits that the invention is an improvement over a previous invention. Generally, a Jepson claim describes the known elements or steps of the previous invention and states “wherein the improvement comprises” or some similar language before proceeding to list the elements or steps that are new or improved over the previous invention (see *Ex parte Jepson* ruled on in 1917).

In Claims 11 and 16, it is stated that PERFORMANCE is improved (i.e., enhanced). But note that it is not an existing prior art that is stated in the claim to be improved (i.e., the claims do not list elements of a previous invention and the elements of the present claims that are novel over the previous invention). Thus, Claims 11 and 16 are not Jepson claims.

Consequently, the objection to Claims 11 and 16 is not warranted. Withdrawal to the objection is kindly requested.

For the reasons stated more fully below, Applicants submit that the claims are allowable over the applied references. Hence, reconsideration, allowance and passage to issue are respectfully requested.

The invention is set forth in claims of varying scopes of which Claim 1 is illustrative.

> 1. A method of improving performance in a multiprocessor system that uses a limited number of physical interfaces to transact network data comprising the steps of:
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> determining whether data being processed is network data; and
>
> ***transacting, if the data is network data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address given to a data holding device in the multiprocessor system***. (Emphasis added.)

Once more, the Examiner rejected the independent claims under 35 U.S.C. §102(e) as being anticipated by Nakashima. Applicants once more respectfully disagree.

Nakashima purports to teach a load-balancing method for a multi-processor system with a plurality of processor modules. In accordance with the purported teachings of Nakashima, the multi-processor system is assigned a virtual IP address while each processor module of the multi-processor system is assigned a real IP address. The virtual IP address is used to direct data to the multi-processor system which then determines which one of the processor

modules is to handle the data. The determination can be made based on the load of each processor module in the system. That is, when a piece of data arrives at the multi-processor system (through the use of the virtual IP address), the system forwards the data to the processor module with the lightest load for processing.

The virtual IP address of the multi-processor system and the real IP address of each module are correlated and stored for easy access by a router. This allows the router to send data to the multi-processor system using the virtual IP address when the data contains the real IP address of one of the processor modules of the multi-processor system (see paragraph [0028]).

However, Nakashima does not teach, show or so much as suggests the step of ***transacting, if the data is network data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address given to a data holding device in the multiprocessor system*** of the claimed invention.

On page 3 of the Action, the Examiner stated that:

> The Examiner agrees with Applicant's argument that "*Nakashima teaches the virtual IP addresses and indeed IP addresses in general are assigned to the processor modules and the system*" (see page 10). However, since the disclosure does not further define what a data holding device may entail, the Examiner considers the processor modules are [sic] indeed data holding devices.

Firstly, a processor module is used to process data and not to hold data. Therefore, a processor module is a processing device not a "data holding device."

Secondly, whether or not the disclosure further defines a data holding device is irrelevant. What is relevant are the claimed limitations. Here, the claims specifically include the limitations of ***transacting, if the data is network***

data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address given to a data holding device in the multiprocessor system. The claims do not include the limitations of a *virtual IP address being given to a processor module*.

Note, nonetheless, that because "data holding devices" are so ***well known in the field***, there is not any reason for a requirement that they be further defined.

Note further that the claimed limitations include a MULTIPROCESSOR SYSTEM and yet state that the virtual IP address is given to a "data holding device" and not to the processor(s) of the multiprocessor system. Therefore, the Examiner cannot substitute "processor module" for "data holding device" in the claims.

Thirdly, although irrelevant, the argument that the disclosure does not further define a "data holding device" is disingenuous. "Data holding devices" are not novel devices and are very well known in the field to include buffers. Page 11, line 14 to page 13, line 5 and Fig. 5 have been devoted to buffers and their variants. Therefore, the disclosure has ample definition of a "data holding device."

Fourthly, Nakashima specifically teaches that real IP addresses are assigned to the processor modules while a virtual IP address is assigned to the multiprocessor system. If one were to agree with the Examiner's assertion that the processor modules are indeed "data holding devices," then in order for the teachings of Nakashima to anticipate the claimed invention, virtual IP addresses would be assigned to the processor modules. This is in direct contradiction to the teachings of Nakashima that require that real IP addresses be assigned to the processor modules so that data can be routed appropriately to the system.

Based on the foregoing, Applicants submit that Nakashima does not anticipate the independent claims in the Application as asserted by the Examiner.

The Examiner rejected the dependent claims (i.e., Claims 2 – 5, 7 – 10, 12 – 15 and 17 – 20) under 35 USC §103(a) as being unpatentable over Nakashima

in view of Acharya et al. Applicants submit that the teachings of Nakashima can not be combined with those of Acharya et al. to show or to render the claimed invention obvious.

As mentioned above, Nakashima teaches the step of assigning a virtual IP address to a multiprocessor system that has a plurality of processor modules while assigning real IP addresses to the processor modules. When data is addressed to a processor module via the processor module's real IP address, a router substitutes the virtual IP address of the multiprocessor system for the real IP address of the processor module. Since the data is now addressed to the multiprocessor system instead of to a particular processor module, the multiprocessor system, upon receiving the data, can forward the data to any one of the processor modules. In this case, the multiprocessor system forwards the data to the least used processor module in order to load-balance the system.

By contrast, Acharya et al. teach a method of virtualizing iSCSI storage. According to Acharya et al., each physical storage device supports multiple logical units (LUNs) and each supported LUN is associated with a separate TCP port number. ISCSI commands received on a given port implicitly refer to the associated LUN. An iSCSI host addresses each logical unit of storage (LUN) with a virtual IP address and port number. Using an address translation table, a virtualization gateway rewrites the destination IP address in the header of an incoming packet as well as the destination port number to correspond to the target physical LUN. Migration of logical units across physical storage devices is supported by changing the address translation entries at the gateway; and the gateway can be provided by a standard network router with support for address translation.

Thus, Nakashima advocates substituting virtual IP addresses for real IP addresses when transacting data while Acharya et al. advocate substituting real IP addresses for virtual IP addresses when transacting data. Therefore, they each teach away from the other.

It has repeatedly been held that references that teach away from each other cannot serve to create a prima facie case of obviousness. *In re Gurley*, 27 F.3d 551, 553, 31 USPQ 2d 1130 (Fed. Cir. 1994), in *McGinley v. Franklin Sports Inc.*, 60 USPQ 2d 1001, 1010 (Fed. Cir. 2001). See also *KSR International Co. v. Teleflex Inc.*, 550 U.S. ____, 82USPQ2d 1385 (2007).

Since, in this case Nakashima teaches away from Acharya et al., Applicants submit that the claims are not obvious in view of the applied references.

Consequently, Applicants once more respectfully request reconsideration, allowance and passage to issue of the claims in the Application.

Respectfully Submitted

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